"A Data-Parallel Programming Model for Reconfigurable Architectures"

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Overview

- Reconfigurable Architectures
- Programming Model
- Compiling an Example

Reconfigurable Architectures: FPGAs

Example: Xilinx 4010

- 20x20 matrix of CLBs and Routing support
- 10,000 gates, 1120 flip/flops, 12,800 bits SRAM, 160 I/O pins
- Implementing Devices
  - 24 bit Accumulator: 13 CLBs, 32 ns
  - 16:1 MUX: 5 CLBs, 16 ns
  - 16 bit adder: 9 CLBs, 20.5 ns
- Programmable in-circuit in milliseconds

Reconfigurable Architectures: Machines

Example: Virtual Computer

- Attached Processor for Workstations
- Logic Pipelines composed of SRAM, XC4010s, ICUBE communication ASICs
- Configuration Control

Programming Model: Motivation and Vectors

- Motivation: Want to do large amounts of work between reconfigurations, but minimize reconfiguration time

- Vector model
  - Can configure any possible type of vector functional unit
  - Deep pipelines
  - Long vectors

- But data dependencies limit pipeline depth

Programming Model: Vector-based Data Parallel Model

- Elliminate data dependencies by only supporting data parallel semantics - "All operation are performed in parallel on a vector of data"

- Solution: data parallel semantics on top of a vector implementation

- Extend with scan primitives

- Result: C with vector operators and function calls to scan primitives

Compiling an Example

$$e^x - 1 = x + x^2/2! + x^3/3! \ldots$$

- Form data flow graph
- Replace computations with functional units
- Insert delay stages correctly when merging pipelines (paths through graph)
- Give this RTL representation to synthesis and routing tools
- Use optimizations like common subexpression elimination and strength reduction to reduce logic

What wasn't covered

- Claim to have coded several algorithms to this model, but don't present any results
- Don't talk about pipelining within individual functional units
- How to deal with a data flow graph that exceeds logic and pin resources?